10/ Chitwood 2/5/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Takaaki NAGAI et al.

Title: EEPROM SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Appl. No.: 09/606,159

Filing Date: 06/29/2000

Examiner: P. Brock, II

Art Unit: 2815



AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.116

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed May 11, 2001, please amend the above-identified application as follows:



IN THE CLAIMS:

Please enter the following amended claims:

21. (Twice Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a later formed plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon strips in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

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